Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1–11. (canceled)

12. (previously presented) A clock control system for generating a clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature, comprising:

a thermal sensor operative to produce a temperature signal corresponding to a junction temperature of at least a portion of a circuit on a die;

a thermal sensor control circuit, operatively coupled to the thermal sensor, and operative to produce temperature data in response to the temperature signal and to provide an interrupt control signal in response to the temperature data;

a clock generator circuit operative to produce the clock signal; and

a dynamic overclock frequency control data generator, operatively coupled to the thermal sensor control circuit and the clock generator circuit, and operative to provide dynamic overclock frequency control data to the clock generator circuit in response to the interrupt control signal and the received temperature data to cause the clock generator circuit to increase the operating frequency of the clock signal above the nominal operating frequency, when the detected junction temperature is less than the maximum rated junction temperature.

13. (previously presented) The clock control system of claim 12 wherein the dynamic overclock frequency control data generator is operative, in response to the interrupt control signal, to provide hysteresis based frequency control to increase the operating frequency of the

clock signal above the nominal operating frequency if the detected junction temperature is below a lower junction temperature threshold, and to decrease operating frequency of the clock signal below the nominal operating frequency if the detected junction temperature is above an upper junction temperature threshold, wherein the upper junction temperature threshold is greater than the lower junction temperature threshold.

14. (canceled)

15. (previously presented) The clock control system of claim 12 wherein the thermal sensor control circuit is operative to produce the interrupt control signal in response to a comparison between the temperature data and threshold temperature data.

16. (previously presented) The clock control system of claim 12 wherein the dynamic overclock frequency control data generator is operative to reduce at least one of: the frequency of the clock signal and a supply voltage to at least the portion of the circuit on the die in response to the interrupt control signal and if the detected junction temperature is above a junction temperature threshold.

17. (previously presented) In a system comprising a host processor and a graphics co-processor, a method for generating a clock signal for the graphics co-processor, the clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature, the method comprising:

detecting, by a thermal sensor coupled to the graphics co-processor, a junction temperature corresponding to at least a portion of a circuit on a die constituting at least a portion of the graphics co-processor, thereby providing a temperature signal;

providing, by a thermal sensor control circuit coupled to the thermal sensor, an interrupt control signal and temperature data in response to the temperature signal; and

causing, by the host processor coupled to the thermal sensor control circuit and in response to the interrupt control signal and the temperature data, an increase in the operating frequency of the clock signal above the nominal operating frequency, when the detected junction temperature is below the maximum rated junction temperature.

18. (previously presented) The method of claim 17 further including decreasing, by the host processor in response to the interrupt control signal, the operating frequency of the clock signal below the nominal operating frequency when the detected junction temperature is above the maximum rated junction temperature.

19. (previously presented) The method of claim 18 further including providing hysteresis based frequency control by:

decreasing, by the host processor in response to the interrupt control signal, the operating frequency of the clock signal if the detected junction temperature is above an upper junction temperature threshold, and

increasing, by the host processor in response to the interrupt control signal, the operating frequency of the clock signal if the detected junction temperature is below a lower junction

temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold.

20–33. (canceled)

34. (previously presented) A clock control system for generating a clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature, comprising:

a thermal sensor operative to produce a temperature signal corresponding to a junction temperature of at least a portion of a circuit on a die;

a thermal sensor control circuit, operatively coupled to the thermal sensor, and operative to produce temperature data in response to the temperature signal and to provide an interrupt control signal in response to the temperature data;

a clock generator circuit operative to produce the clock signal;

a dynamic overclock frequency control data generator, operatively coupled to the thermal sensor control circuit and the clock generator circuit, and operative to provide dynamic overclock frequency control data to the clock generator circuit in response to the interrupt control signal and the received temperature data to cause the clock generator circuit to increase the operating frequency of the clock signal above the nominal operating frequency, when the detected junction temperature is less than the maximum rated junction temperature; and

memory comprising data representing junction temperatures over a temperature operating range with corresponding clock signal frequencies.

35.-36. (canceled)

37. (previously presented) The clock control system of claim 16, wherein the junction temperature threshold is the maximum rated junction temperature.

38. (previously presented) The clock control system of claim 34, wherein the data representing junction temperatures over the temperature operating range with corresponding clock signal frequencies are organized as at least one lookup table.

39. (previously presented) The clock control system of claim 34, wherein the dynamic overclock frequency control data generator is further operative to provide dynamic overclock frequency control data to the clock generator circuit to the clock generator circuit in response to the temperature data and the interrupt control signal to cause the clock generator circuit to decrease the operating frequency of the clock signal below the nominal operating frequency, when the detected junction temperature is greater than the maximum rated junction temperature.

40. (previously presented) The clock control system of claim 34, wherein the thermal sensor control circuit is operative to produce the interrupt control signal in response to a comparison between the temperature data and threshold temperature data.

41. (previously presented) The clock control system of claim 34, wherein the data representing at least the clock signal frequencies account for a predetermined physical installation of the circuit on the die.

42. (previously presented) The clock control system of claim 34, wherein the data representing at least one of the junction temperatures and corresponding clock signal frequencies are based on a qualification testing procedure and further includes a safety margin to avoid a thermal runaway condition.

43. (previously presented) The clock control system of claim 34, wherein at least one of the dynamic overclock frequency control data generator and the thermal sensor control circuit is further operative to determine a processing load on the circuit on the die and to provide the dynamic overclock frequency control data to the clock generator circuit in response to the temperature data, the interrupt control signal and the processing load.

44. (previously presented) The clock control system of claim 34, wherein the dynamic overclock frequency control data further cause the clock generator circuit to reduce a supply voltage to at least the portion of the circuit on the die, when the detected temperature is greater than the maximum rated junction temperature.

45. (previously presented) A clock control system for generating a clock signal having an operating frequency set to a first frequency corresponding to a first junction temperature, comprising:

a thermal sensor operative to detect a junction temperature corresponding to at least a portion of a circuit on a die;

a temperature dependent dynamic overclock generator circuit, operatively coupled to the thermal sensor, and operative to increase the operating frequency of the clock signal above the nominal operating frequency, when the detected junction temperature is below the maximum rated junction temperature; and

memory comprising data representing junction temperatures over a temperature operating range with corresponding clock signal frequencies, wherein the data representing junction temperatures over a temperature operating range with corresponding clock signal frequencies account for a predetermined physical installation of the circuit on the die.

46. (previously presented) The clock control system according to claim 45, wherein the data representing at least one of the junction temperatures and the corresponding clock signal frequencies are based on a qualification testing procedure and further includes a safety margin to avoid a thermal runaway condition.

47. (currently amended) A clock control system for generating a clock signal having an operating frequency set to a first frequency corresponding to a first junction temperature, comprising:

a thermal sensor operative to detect a junction temperature corresponding to at least a portion of a circuit on a die;

a temperature dependent dynamic overclock generator circuit, operatively coupled to the thermal sensor, and operative to increase the operating frequency of the clock signal above the

nominal operating frequency, when the detected junction temperature is below the maximum rated junction temperature; and

memory comprising data representing junction temperatures over a temperature operating range with corresponding clock signal frequencies, wherein the data representing junction temperatures over a temperature operating range with corresponding clock signal frequencies account for a predetermined physical installation of the circuit on the die, and

~~The clock control system according to claim 45, wherein the data representing junction temperatures over a temperature operating range with corresponding clock signal frequencies~~ are organized as at least one lookup table.